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A Sinusoidal Pulse Width Modulation (SPWM) Technique for Capacitor Voltage Balancing of Nested T-Type Four-Level Inverter

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Abstract— In this letter, a new control method based on sinusoidal pulse width modulation(SPWM) scheme is proposed to control capacitor voltages of a four-level T-type NNPC inverter. Four-level T-type NNPC inverter has a lower number of switches and components compare with other four-level classic and advanced inverters which make this topology attractive for high-power medium-voltage applications. This topology has been proposed and studied with the assumption of constant dc sources instead of flying capacitors. In this letter, a simple single-phase modulator is developed to balance flying capacitor voltages. Performance and the feasibility of the proposed control technique are evaluated experimentally at steady-state and transient conditions and for different modulation indices and loads. The experimental results demonstrate the effectiveness of the developed control method to control the capacitors' voltages.

Keywords— *Multilevel Converters, capacitor voltage balancing, T-type structure, sinusoidal pulse width modulation* (*SPWM*)

I. Introduction

Multilevel inverters are very attractive and commonly used for high-power medium-voltage applications [1]-[2]. Neutral-point clamped (NPC) converter, flying capacitors (FC) converter and the cascaded H-bridge (CHB) converter are classical multilevel converters [3]. However, these classic topologies have some disadvantages which limit their applications. For NPC topologies, voltage balancing of the dc-link capacitors is a challenge especially for a higher number of levels. The number of clamping diodes also increases significantly with the higher number of levels. For FC topology, the higher switching frequency is needed in order to keep the capacitor voltages balanced. Also, FC topology in a higher number of levels has a higher number of capacitors which reduces the reliability and lifetime of the converter. Cascaded H-bridge has a modular structure which can get higher voltages and number of levels with increasing the number of cells. However, CHB topology needs several isolated dc sources provided by a bulky, expensive phase-shifting transformer. The number of switches in CHB topology increases significantly in a higher number of output levels [1]–[3].

Advanced multilevel topologies have been presented and some of them have been manufactured [4]-[15]. Most of the new topologies are combinations of the main classic topologies which tries to eliminate or mitigate the disadvantages of the classic topologies. A various number of these new multilevel topologies are being used in industry; five-level H-bridge NPC (5L-HNPC), the three-level active NPC (3L-ANPC), and the five-level active NPC (5L-ANPC).

The H-bridge connection of two classic 3-level NPC presents a 5-Level HNPC converter that can operate at higher voltage levels than a conventional NPC converter. However, this topology needs a number of isolated dc sources provided by a bulky and expensive phase-shifting transformer [5]-[7]. One of the disadvantages of NPC converter is the unequal losses between the inner and outer switching devices.

A 3-level active NPC (ANPC) is a topology that clamping switches are replaced with clamping diodes and provide a controllable path for neutral current and thus loss distribution between switches is balanced [8]-[11]. However, the number of active switches is increased compared to a conventional NPC converter which increases the cost of producing the converter and decreases the reliability of the converter.

5- level active NPC, which can generate a higher number of levels and improve the output voltage quality, is a combination of 3-level ANPC and 3-level FC. However, in a 5-level ANPC voltage rating of the switches are different [12]-[14]. A four-level nested neutral point clamped (4L-NNPC) converter is presented in [15]-[16]. This topology has a fewer number of components compared to the existing topologies.

Recently, a new four-level T-type NNPC has been proposed in [17], shown in Fig,1. The Nested T-Type four-level NNPC is very attractive for high-power and medium-voltage applications due to the lower number of devices as compared with other 4-level topologies in Table I.

TABLE I: Comparison Number of Devices Among Different Topologies

Topology	Number of switches	Number of clamping diodes	Number of flying capacitors
NPC	18	18	-
FC	18	-	9
NNPC	18	6	6
T-Type NNPC	**18**	**-**	**6**

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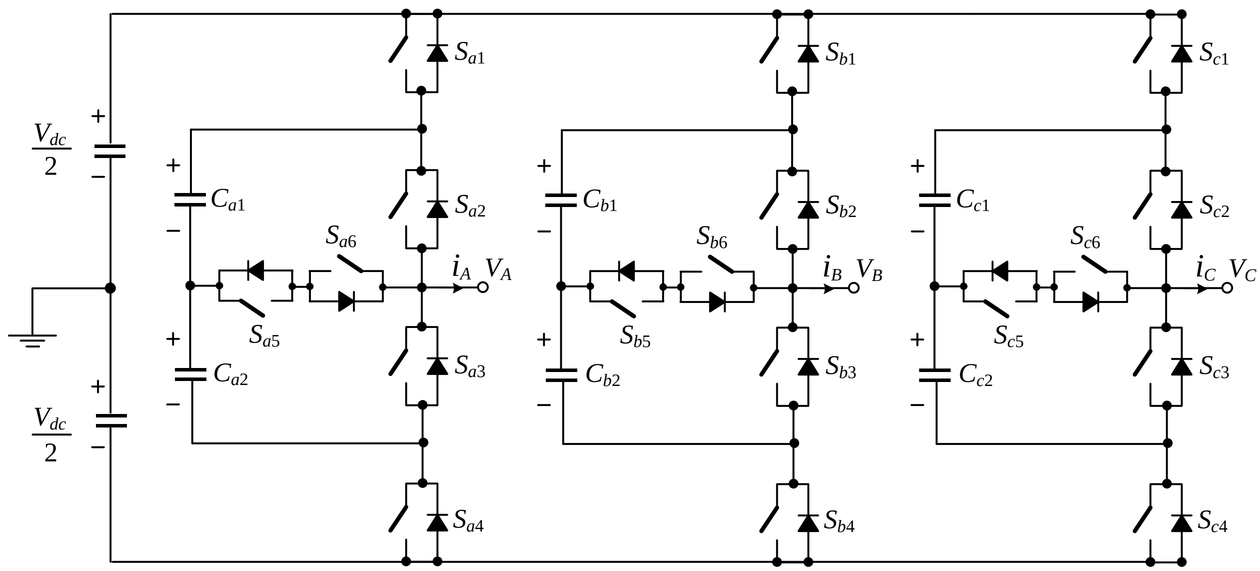

Fig. 1. Nested T-type four-level nested neutral point clamped (T-NNPC) Inverter [17]

As can be seen from the Table I, T-type NNPC has lower number of components and thus the size, weight, cost, and reliability of the converter has been improved compared to the existing four-level topologies The operation of the inverter is studied in [17], with assumption of constant dc sources instead of flying capacitors, which is not practical. In practice, the flying capacitors are employed instead of dc sources, so a more sophisticated control method is required to regulate the flying capacitor voltages. In this letter, a new control method based on sinusoidal pulse width Modulation (SPWM) is developed to control and balance the voltages of flying capacitors at the desired voltage level and thus the T-type NNPC can operate properly at different operation conditions.

The performance of the developed control strategy is studied in the MATLAB/Simulink environment and verified experimentally at steady-state and transient conditions and for different modulation indices.

In Section II, the T-type NNPC operation is explained briefly and then sinusoidal pulse width modulation will be used to control flying capacitor voltages. In Section III, the proposed control technique is developed. In Section IV, the feasibility and performance of the proposed controller are verified experimentally.

II. Operation of The Nested T-Type Neutral Point Clamped Inverter

A four-level T-type NNPC topology is a combination of a flying capacitor topology and a T-type inverter [17]. The capacitor C_{x1} and C_{x2}, $x = a,b,c$ are charged to one-third of the total DC-link voltage. Six switching states can generate four output voltage levels as can be seen in Table II. A controllable current path is provided by the bidirectional switches to control the direction of the output current. As shown in Table II, level 2 and level 3 have two redundant switching state which generates medium voltage level $1/6V_{dc}$ and $-1/6V_{dc}$ respect to the mid-point of the dc source.
Each of these redundant switching states has a specific charging and discharging effect for each flying capacitor. The method for controlling the capacitors' voltages is based on choosing the best redundant switching state which makes the capacitor charge or discharge to the desired voltage which is one-third of total DC-link voltage.

III. Sinusoidal Pulse Width Modulation for a T-Type NNPC Converter

Capacitor voltage balancing of a T-Type NNPC converter is a technical challenge to make sure that the converter can operate properly under different operating conditions. If there is no control, the flying capacitors will be charged or discharged during the converter operation and the capacitors' voltages will deviate from the desired values and thus the converter cannot generate a four-level output voltage. In this Section, a new control technique based on SPWM scheme is explained.
The deviation of the capacitor voltages from the desired value (V_{dc} / 3) can be written as:

$$\Delta V_{Cxi} = V_{Cxi} - V_{dc}/3$$
$$x = a,b,c \quad i = 1,2$$

In order to balance the capacitor voltages, ΔV_{CXi} (x=a,b,c, i=1,2) should be zero or close to zero at all operating conditions. If the voltage deviation is positive, a switching state should be selected to discharge the capacitor and if the deviation is negative, the switching state should be selected to charge the capacitor.

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TABLE II: SWITCHING STATES OF THE T-TYPE FOUR-LEVEL INVERTER AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO THE FLYING CAPACITOR VOLTAGES

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{Cx1}	V_{Cx2}	V_{xn}	Output Level	State
1	**1**	**0**	**0**	**1**	**0**	No Impact	No Impact	$\frac{V_{dc}}{2}$	3	3
1	**0**	**0**	**0**	**1**	**1**	Charging (ix>0) Discharging (ix < 0)	No Impact	$\frac{V_{dc}}{6}$	2	2B
0	**1**	**0**	**1**	**1**	**0**	Discharging (ix > 0) Charging (ix < 0)	Discharging (ix > 0) Charging (ix< 0)			2A
1	**0**	**1**	**0**	**0**	**1**	Charging (ix >0) Discharging (ix < 0)	Charging (ix > 0) Discharging (ix < 0)	$-\frac{V_{dc}}{6}$	1	1B
0	**0**	**0**	**1**	**1**	**1**	No Impact	Discharging (ix > 0) Charging (ix< 0)			1A
0	**0**	**1**	**1**	**0**	**1**	No Impact	No Impact	$-\frac{V_{dc}}{2}$	0	0

TABLE III: THE PROPOSED VOLTAGE CONTROL METHOD

Output Level	i_x	ΔV_{CX1}	ΔV_{CX2}	Condition	State
1	≥ 0	≥ 0	≥ 0	-	1A
			< 0	-	1B
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	1A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	1B
			< 0	-	1B
	< 0	≥ 0	≥ 0	-	1B
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	1A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	1B
		< 0	≥ 0	-	1B
			< 0	-	1A
2	≥ 0	≥ 0	≥ 0	-	2A
			< 0	-	2A
		< 0	≥ 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	2A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	2B
			< 0	-	2B
	< 0	≥ 0	≥ 0	-	2B
			< 0	$\lvert\Delta V_{CX1}\rvert < \lvert\Delta V_{CX2}\rvert$	2A
				$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	2B
		< 0	≥ 0	-	2A
			< 0	-	2A

However, as it can be seen from Table II, for some switching states, capacitors of a phase are jointly charged and discharged which is a challenge for controlling the capacitor voltages. For example, assuming the voltage level is 1, if the deviation for C_1 is positive and the deviation of C_2 is negative, and the output current is larger than zero, choosing 1A will charge C_2 toward the the desired value but also it charges C_1 more, and deviation for C_1 will increase, which is not desirable.

To solve this problem, Table III is developed that shows the procedure of selecting the best switching state to balance the capacitors voltages at desired values. For level 0 and 3, there is no redundant switching state and these two levels do not affect the capacitor voltages. However, for level 1 and 2, there are redundant switching states and based on the current direction and voltage deviation of the capacitors, the best switching states will be selected from Table III.

For instance, when the output voltage level is 1, and $i_x \geq 0$, $\Delta V_{Cx1} \leq 0$, $\Delta V_{Cx2} \leq 0$, both capacitors needs to be charged and thus switching state 1B should be selected.

The flowchart shown in Fig. 2 shows the procedure to control voltage of flying capacitors in each phase:

- First, by comparing carriers (three carriers for a four-level converter) and the modulation signal, desired output voltage level is determined.
- The direction of the phase currents and capacitor voltages should be measured.
- Based on the output voltage level, the current direction and capacitor voltage deviations, proper switching state will be selected from Table III.
- And finally, the gate signals are generated and applied to the switching devices.

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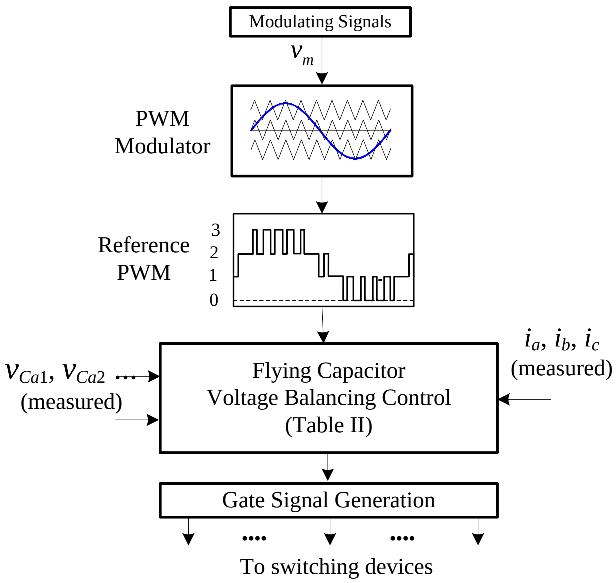


Fig. 2. Block diagram of capacitor voltage balancing control

IV. Experimental Results

The feasibility of the proposed control technique based on SPWM scheme is evaluated experimentally. The parameters shown in Table IV are used to obtain the experimental results from a scaled-down prototype.

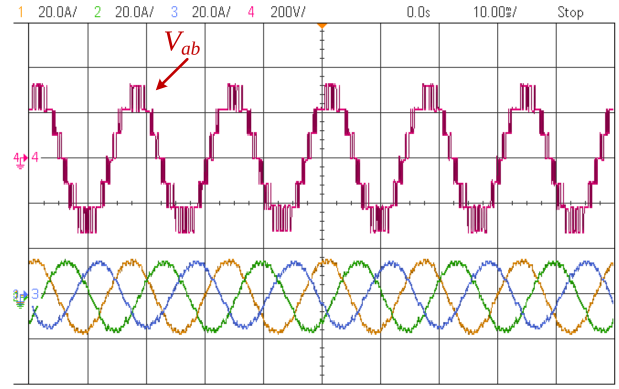
Fig. 3 to 6 show the performance of the proposed control technique under steady-state and transient conditions. Fig. 3 shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.9 and load PF=0.9. The inverter output voltage THD is 24.7%. Fig. 4 also shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.55 and load PF=0.9. The inverter output voltage THD is 40.7%.

Fig. 5 shows the performance of the converter when modulation index changes from m=0.55 to m=0.9.

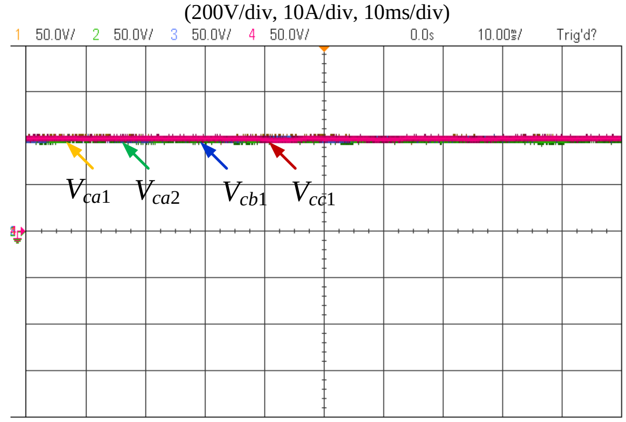
Fig. 6 shows the performance of the controller when the controller is deactivated and activated. Without the controller, capacitors start to diverge and when the controller activated, the capacitor will be converged. As can be seen from Figs. 3 to 6 show the effectiveness of the proposed controller and demonstrate that all capacitor voltages are well balanced at different operating conditions.

TABLE IV: PARAMETERS OF THE STUDY SYSTEM

Converter parameters	Values
Converter rating (kVA)	5
Capacitor Value (μF)	2200
Input dc voltage (V)	320
Output frequency (Hz)	60
Output inductance (mH)	5
Output load (Ω)	12

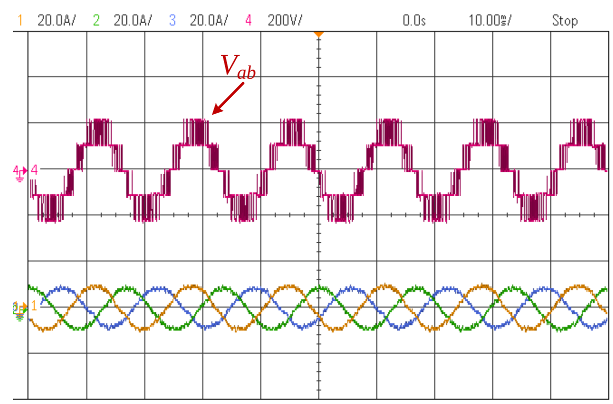


(a) inverter output line voltage and output currents (200V/div, 10A/div, 10ms/div)

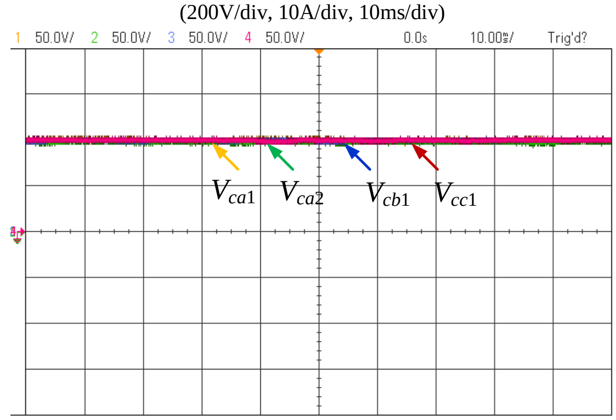


(b) voltages of flying capacitors (50V/div, 10ms/div)

Fig. 3. Experimental results, m = 0.9 and PF=0.9.



(a) inverter output line voltage and output currents (200V/div, 10A/div, 10ms/div)



(b) voltages of flying capacitors (50V/div, 10ms/div)

Fig. 4. Experimental results, m = 0.55 and PF=0.9.

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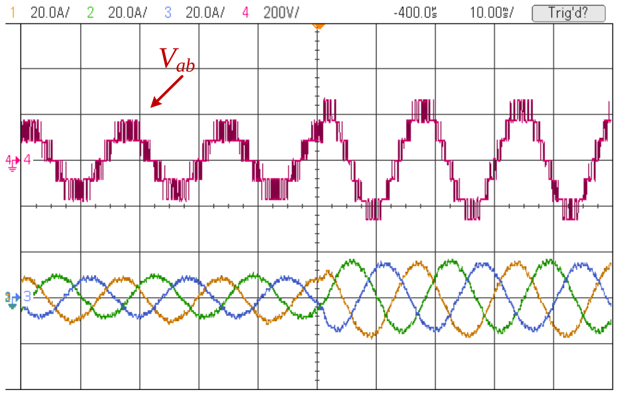
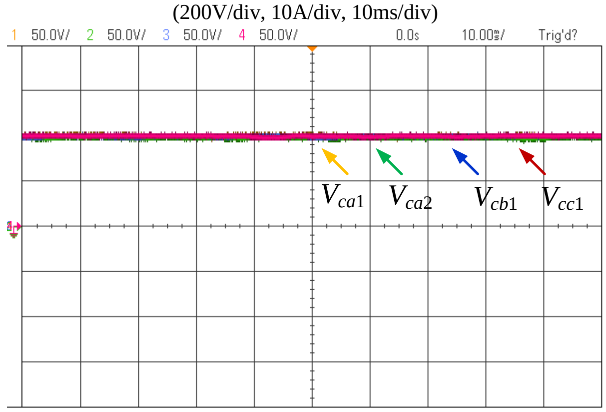


(a) inverter output line voltage and output currents (200V/div, 10A/div, 10ms/div)



(b) voltages of flying capacitors(50V/div, 10ms/div)

Fig. 5. Experimental results, modulation change from m=0.9 to m=0.55.

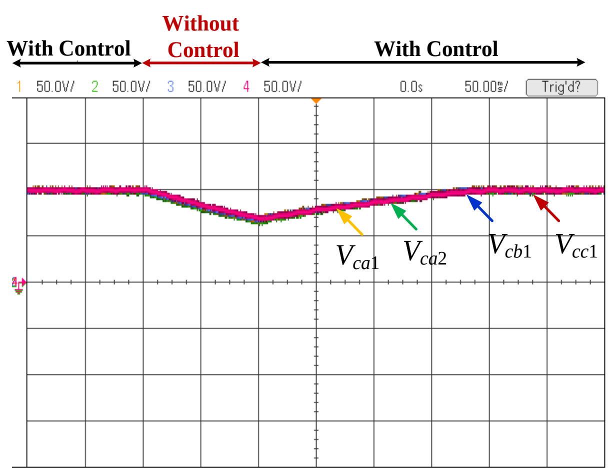


Fig. 6. Voltage of flying capacitor when the controller is deactivated and activated

V. Conclusion

A new method to control flying capacitor voltages of a four-level T-type NNPC inverter base on sinusoidal pulse width modulation(SPWM) is proposed in this letter. This topology is very attractive for medium-voltage applications due to the less number of components compared to the existing topologies. The proposed control method selects the best switching state among the redundant switching states to charge and discharge the flying capacitors and minimize the voltage deviations of the capacitors from the desired values. As the proposed controller is based on SPWM technique, is very simple to implement. The feasibility of the proposed control technique is evaluated by simulation studies and experimentally. The results demonstrate the effectiveness of the proposed technique.

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